EFFECT OF DEVICE LAYOUT ON THE THERMAL RESISTANCE OF HIGH-POWER THERMALLY-SHUNTED HETEROJUNCTION BIPOLAR TRANSISTORS

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Abstract

The effect of device layout on thermal impedance of thermally-shunted HBTs was investigated. A direct comparison of thermally shunted devices and standard airbridge devices is made. Changes in thermal resistance of up to 67% were observed. While thermal resistance remains sensitive to emitter element placement in thermally shunted devices, variations in the location of thermal shunt landings had little effect. These results provide a basis for optimizing thermally-shunted devices.

Introduction

Heterojunction Bipolar Transistors (HBTs) are potentially useful for a number of microwave applications due to their superior power handling capabilities, high linearity, and high gain. Unfortunately, HBTs are susceptible to detrimental self-heating effects (Figure 1) and current distribution instabilities caused by electro-thermal interactions. Current distribution instability manifests itself as a collapse in collector current at high power as current is localized to the hottest finger of the device. (Figure 2). This limitation has made thermal management of HBTs an active area of research [1,2]. Several common thermal management techniques are currently used. For example, base and emitter ballasting [3] are effective techniques to reduce instabilities, but they do not lower the junction temperature. While a flip chip approach [4] lowers junction temperature and stabilizes the device by providing a direct heat sink to the emitter, it is difficult to manufacture. Another novel thermal management technique called thermal shunting, minimizes the HBT junction temperatures and stabilizes the current distribution. The thermal shunt is essentially a thick gold-plated bridge formed between emitter elements that

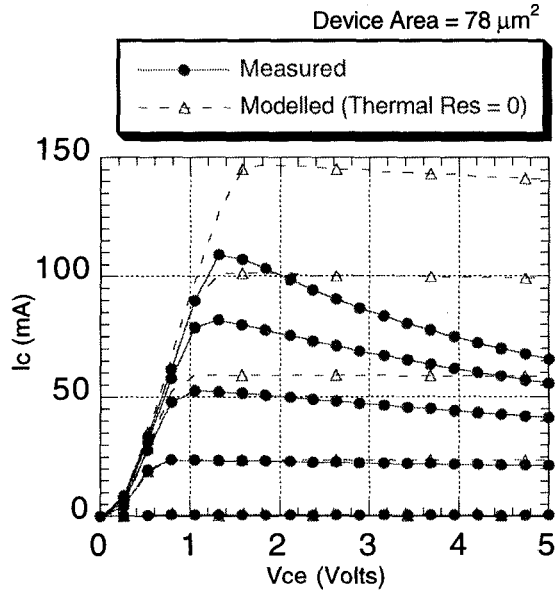

Figure 1 - Measured family of curves showing self-heating effects and same device modelled with zero thermal impedance.

provides a low thermal impedance between the emitters. The area where the thermal shunt comes into contact with the GaAs surface (the thermal shunt landing) provides additional heat sinking for the device. This technique has led to low thermal resistance and record power densities [5]. However, the effect of device layout on the thermal shunt effectiveness has not been determined. This paper presents the results of a preliminary study of these effects. The focus of this study is the effect of emitter element placement and thermal shunt layout on the thermal resistance. These results are significant because they provide the basis to optimize thermal management schemes. Improved thermal management simultaneously permits stable operation at high power due to uniform

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junction temperatures and increased reliability due to reduced junction temperatures.

Device Layout

To investigate the effect of layout on device thermal management, several design variations were included on a single mask set. The significant features of the layout are illustrated in Figure 3. Variations are based on 100 and 200 μm^2 devices. The devices have 4 μm diameter emitter dots with 4 dots per base finger. The 100 and 200 μm^2 devices have two and four fingers respectively. The design variations can be grouped into two categories: changes to the thermal shunt, and changes to the placement of the emitter elements. Changes to the thermal shunt include increasing the shunt span and changing the thermal shunt thickness. Changes to the emitter element placement include changing the separation

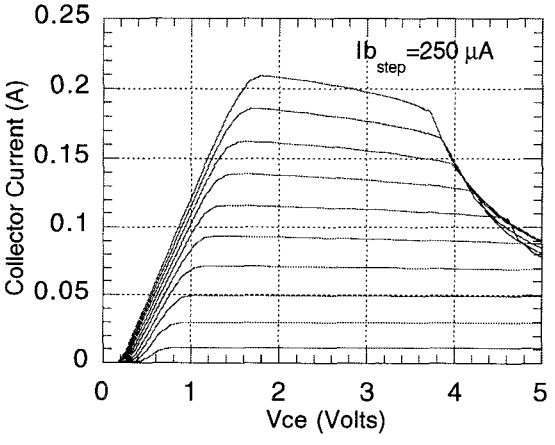

Figure 2. Family of curves for multiple finger HBT showing onset of current collapse.

between emitter fingers and between emitter dots within a finger. The study of separation between emitter fingers was performed on the 4-finger devices. All other variations were based on the 2-finger device. HBTs were fabricated using the Wright Laboratory's thermal shunt process [6].

Thermal impedance was measured using a technique similar to Dawson's method [7,8]. Since the test configuration required a grounded emitter, collector current was forced rather than emitter current. Since the current gains of the devices was greater than 50, the error introduced by using collector current to calculate power is expected to be negligible. Measurements were made on-wafer for two unthinned samples. Values are averages of measurements made on 30 devices across the wafer.

Experimental Results

Of the design variables studied, changes in thermal shunt thickness had the greatest effect followed by the layout of the emitter elements and shunt landing variations. Shunt thickness was investigated by first evaporating 3 μm of gold to connect the emitter elements

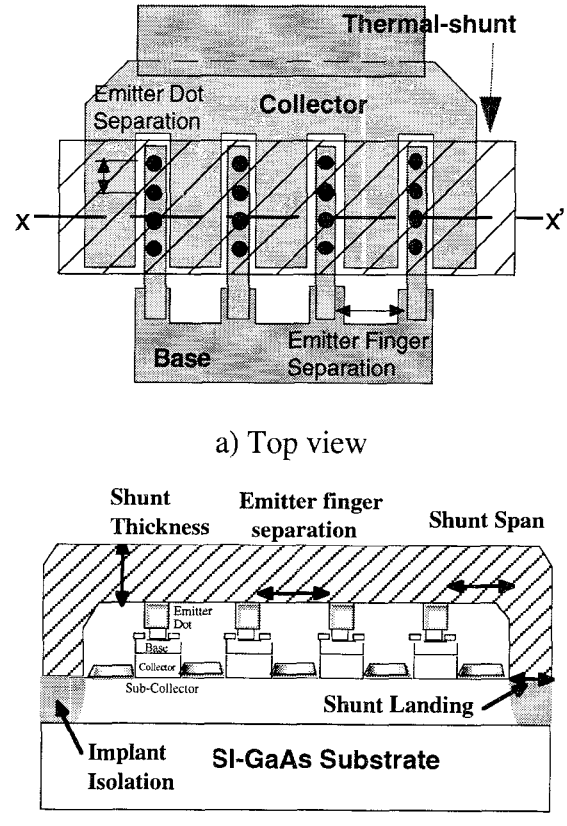

Figure 3. Device Layout

to ground, and then plating an additional 12 μm of gold for selected devices. Measurements indicate a 36% reduction in the thermal resistance by adding the thick thermal shunt to a standard air-bridged 100 μm^2 device on an otherwise identical device layout. In addition, a second sample with a 22 μm thermal shunt was measured. The layout of the device measured on the second sample is identical to that of the first sample. The thermal resistance on this device was 230 °C/W. This value is 67% lower than the standard air-bridge device on sample 1. Similar reductions in thermal resistance were observed for 200 μm^2 devices.

In addition to changes in shunt thickness, emitter element spacing was also investigated. When emitter dot separation was varied from 2 μm to 4 μm within the same

Sample	Shunt Thickness	Device Area (μm^2)	Thermal Resistance °C/W	Percent Change
1	3 μm	100	694	reference
1	15 μm	100	442	-36%
2	22 μm	100	230	-67%
1	3 μm	200	421	reference
1	15 μm	200	278	-34%
2	22 μm	200	162	-65%

Table 1 - Thermal resistance of standard airbridge device and thermally shunted devices

finger, the thermal resistance decreased by approximately 7%. Likewise, when the dot separation was increased from 2 μm to 6 μm, the thermal resistance decreased by 10% (Figure 5). This measurement was repeated on sample 2 with the 22 μm shunt. The second sample, while exhibiting a much lower thermal resistance than sample 1, shows an similar trend with respect to emitter dot

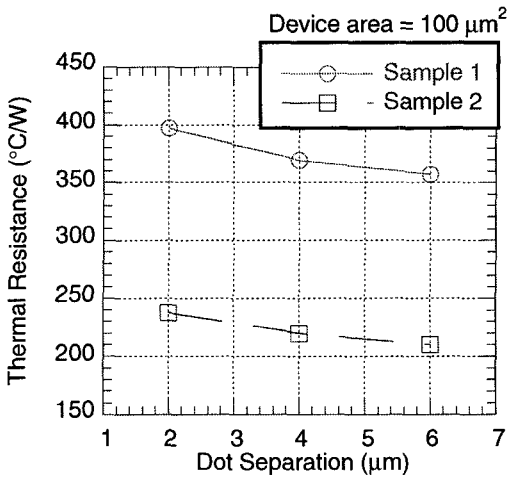

Figure 5 - Thermal Resistance vs. Emitter Dot Separation

separation. Varying the spacing between emitter fingers also showed a significant change. Finger separation was increased from 26 μm to 39 μm as well as decreased to 13 μm and 8 μm. The increased finger separation dropped the thermal resistance by 3% while decreasing the finger spacing resulted in a 9% and 14% increase in thermal resistance (Figure 6). This trend was also matched closely by the second sample with lower thermal impedance. Finally, moving the thermal landings further from the active device area had little effect on the first sample, and almost no effect on the lower thermal impedance sample (Figure 7). Increasing the distance between the emitter elements and the thermal shunt landing by 12 and 24 μm resulted in only a 1.7% and 4.3% increase in thermal resistance in sample 1, respectively. Bringing the landing to within 20 μm of the emitter edge (decreased from 30 μm) decreased the thermal resistance by only 2%.

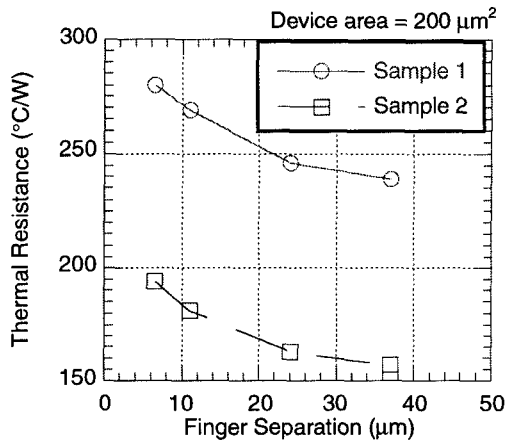

Figure 6 - Thermal Resistance vs. Finger Separation

Conclusions

Thermal resistance was measured for a variety of thermally shunted HBT devices. As a result of this study we have made, for the first time, a direct comparison between devices with and without a thick thermal shunt. We have reduced the thermal impedance by 67% for a 100 μm^2 device by adding a thick thermal shunt. The thermal resistance remains sensitive to the layout of the emitter elements for thermally shunted devices. Changes in emitter dot spacing resulted in a additional 10% decrease in thermal impedance. The thermal resistances are relatively insensitive to changes in the placement of the thermal shunt landing for unthinned samples. Further reductions in thermal resistance are expected when the samples are thinned and backside vias are formed to the shunt landing areas. These results, coupled with an understanding of the RF tradeoffs, permit optimization of thermal management techniques for HBT devices to improve their commercial viability.

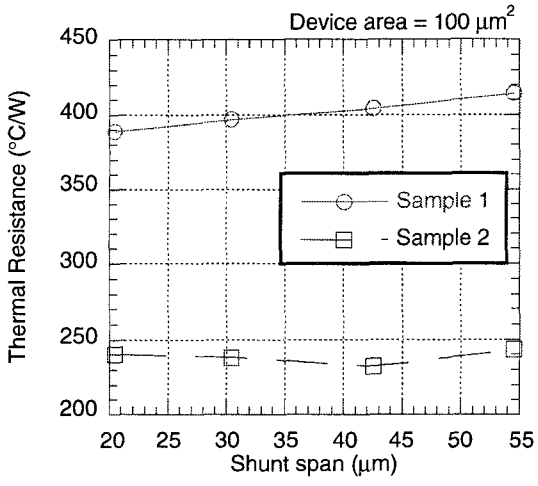

Figure 7 - Thermal Resistance vs. Shunt Span

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